

# MME80R290R

## 800V 0.29Ω N-channel MOSFET

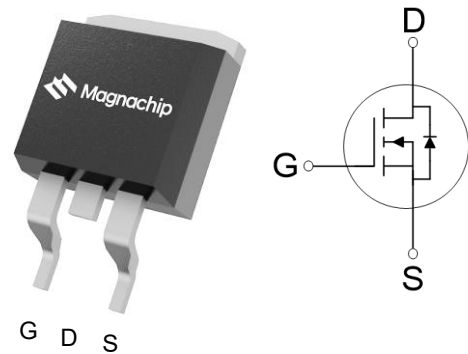
### ■ Description

MME80R290R is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user-friendly devices give an advantage of low EMI to designers as well as low switching loss.

### ■ Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	850	V
$R_{DS(on),max}$	0.29	Ω
$V_{TH,typ}$	3.0	V
$I_D$	17	A
$Q_{g,typ}$	39	nC

### ■ Package & Internal Circuit



### ■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

### ■ Applications

- Flyback power supply stages
- Adapter
- Lighting
- Switching applications

### ■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MME80R290RRH	80R290R	-55 ~ 150°C	D <sup>2</sup> PAK	Reel	Compliant

**■ Absolute Maximum Rating ( $T_c=25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	$V_{DSS}$	800	V	
Gate – Source voltage	$V_{GSS}$	$\pm 30$	V	
Continuous drain current <sup>(1)</sup>	$I_D$	17	A	$T_c=25^\circ\text{C}$
		10.8	A	$T_c=100^\circ\text{C}$
Pulsed drain current <sup>(2)</sup>	$I_{DM}$	51	A	
Power dissipation	$P_D$	255	W	
Single - pulse avalanche energy <sup>(3)</sup>	$E_{AS}$	600	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness <sup>(4)</sup>	dv/dt	15	V/ns	
Storage temperature	$T_{stg}$	-55 ~150	$^\circ\text{C}$	
Maximum operating junction temperature	$T_j$	150	$^\circ\text{C}$	

- 1)  $I_D$  limited by maximum junction temperature
- 2) Pulse width  $t_P$  limited by  $T_{j,max}$
- 3)  $I_{AS} : 3.0 \text{ A}$
- 4)  $I_{SD} \leq I_D, V_{DS\ peak} \leq V_{(BR)DSS}$

**■ Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	$R_{thjc}$	0.49	$^\circ\text{C/W}$
Thermal resistance, junction-ambient max	$R_{thja}$	18.6	$^\circ\text{C/W}$

**■ Static Characteristics (T<sub>c</sub>=25°C unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	V <sub>(BR)DSS</sub>	800	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	2	3	4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> = 800V, V <sub>GS</sub> = 0V
Gate Leakage Current	I <sub>GSS</sub>	-	-	100	nA	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V
Drain-Source On State Resistance	R <sub>DS(ON)</sub>	-	0.25	0.29	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 11A

**■ Dynamic Characteristics (T<sub>c</sub>=25°C unless otherwise specified)**

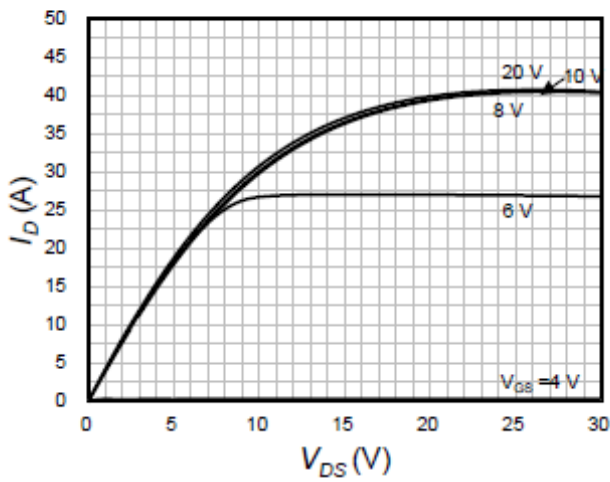
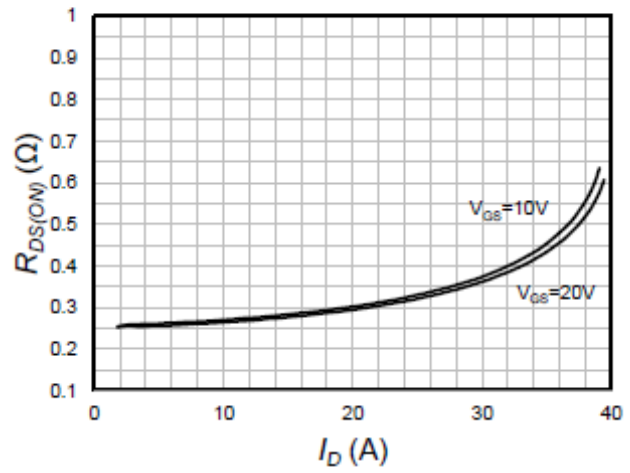
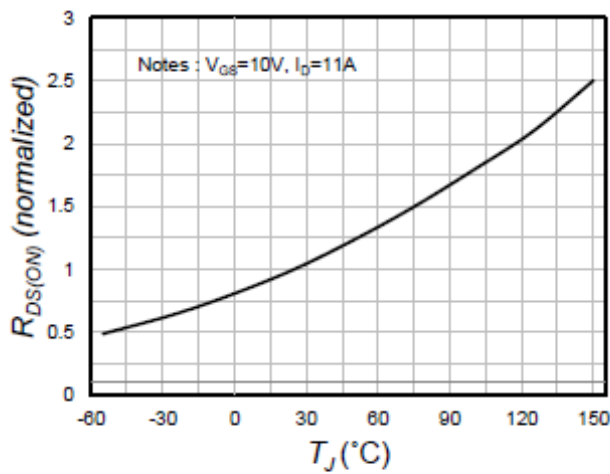
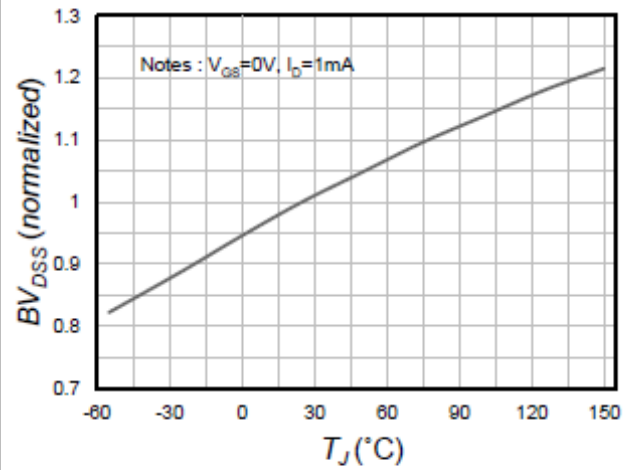
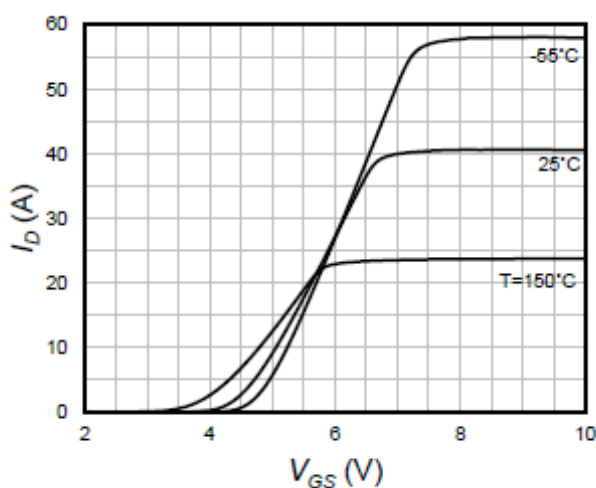
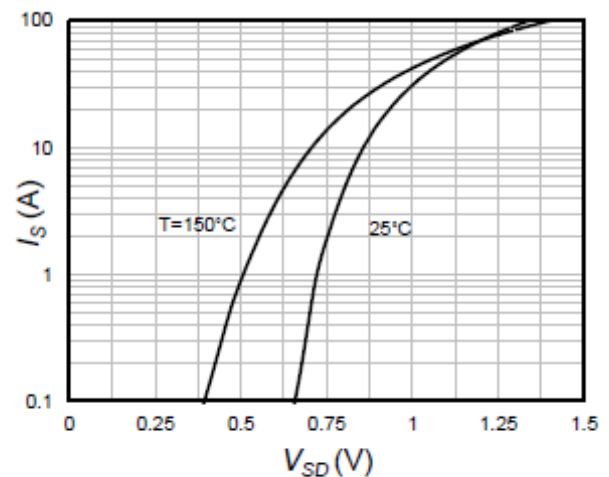
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C <sub>iss</sub>	-	1414	-	pF	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V, f = 400kHz
Output Capacitance	C <sub>oss</sub>	-	29.7	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	3.8	-		
Effective Output Capacitance Energy Related <sup>(5)</sup>	C <sub>o(er)</sub>	-	43.7	-		
Effective Output Capacitance Time Related <sup>(6)</sup>	C <sub>o(tr)</sub>		240			V <sub>DS</sub> = 0V to 640V, V <sub>GS</sub> = 0V, f = 400kHz
Turn On Delay Time	t <sub>d(on)</sub>	-	28	-	ns	V <sub>GS</sub> = 10V, R <sub>G</sub> = 25Ω, V <sub>DD</sub> = 400V, I <sub>D</sub> = 17A
Rise Time	t <sub>r</sub>	-	50	-		
Turn Off Delay Time	t <sub>d(off)</sub>	-	129	-		
Fall Time	t <sub>f</sub>	-	44	-		
Total Gate Charge	Q <sub>g</sub>	-	39	-	nC	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 640V, I <sub>D</sub> = 17A
Gate – Source Charge	Q <sub>gs</sub>	-	7.3	-		
Gate – Drain Charge	Q <sub>gd</sub>	-	19.2	-		
Gate Resistance	R <sub>G</sub>	-	5.3	-	Ω	V <sub>GS</sub> = 0V, f = 1MHz

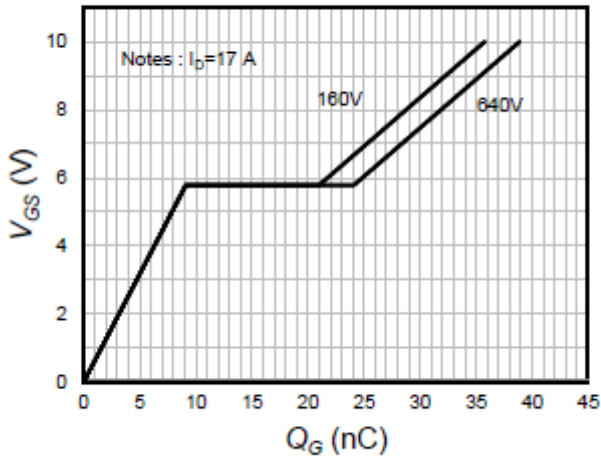
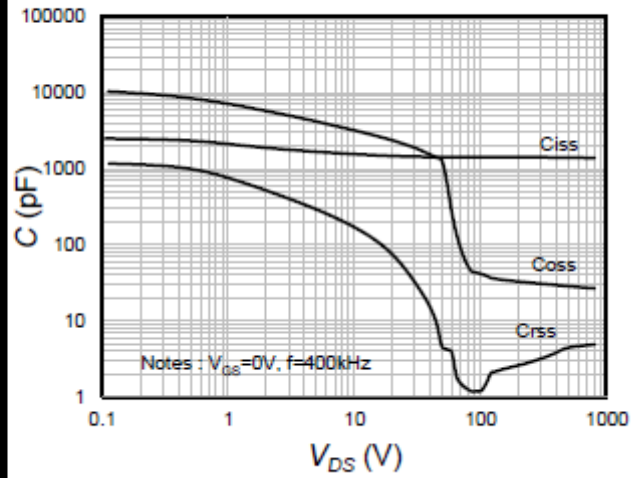
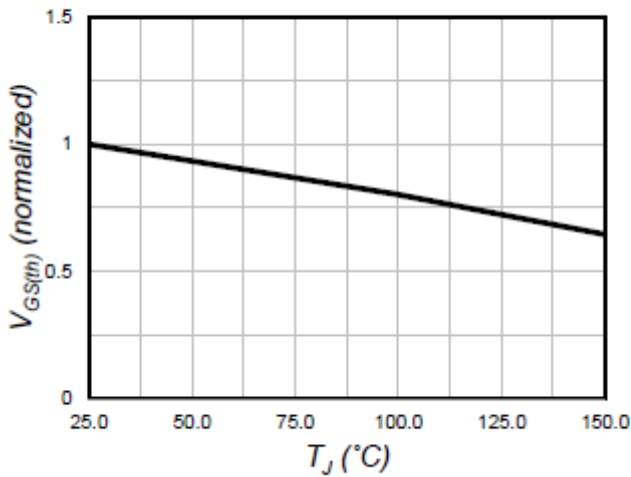
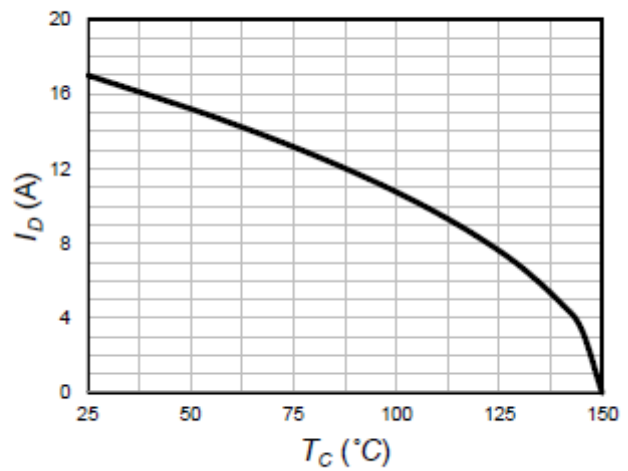
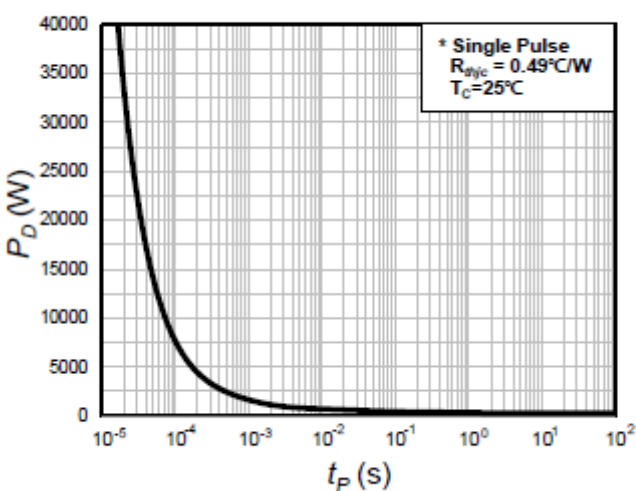
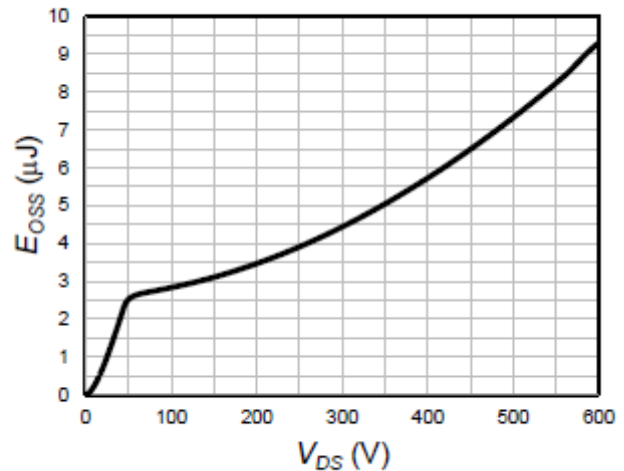
5) C<sub>o(er)</sub> is a capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0V to 80% V<sub>(BR)DSS</sub>

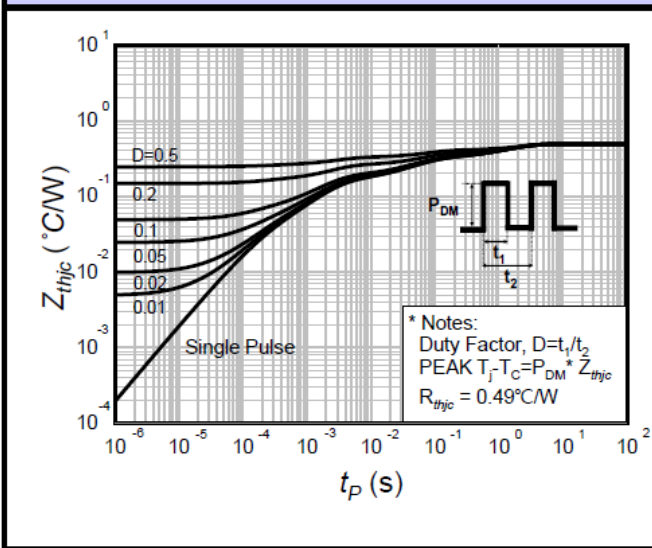
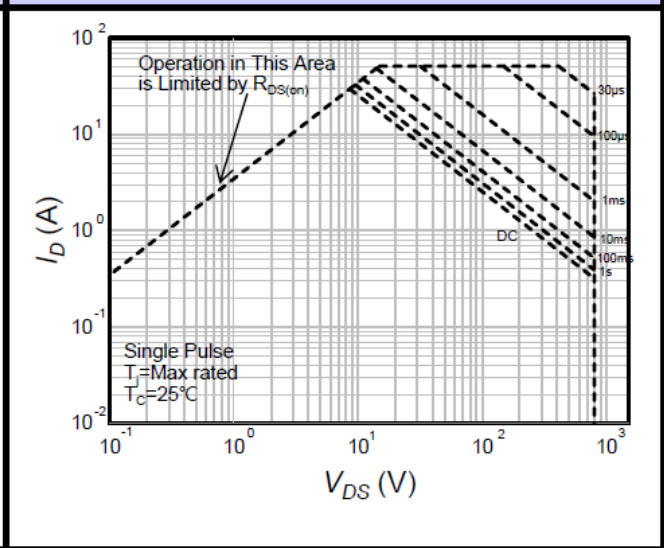
6) C<sub>o(tr)</sub> is a capacitance that gives the same stored charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0V to 80% V<sub>(BR)DSS</sub>

**■ Reverse Diode Characteristics ( $T_c=25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	$I_{SD}$	-	-	17	A	
Diode Forward Voltage	$V_{SD}$	-	-	1.4	V	$I_{SD} = 17\text{A}$ , $V_{GS} = 0\text{V}$
Reverse Recovery Time	$t_{rr}$	-	466	-	ns	$I_{SD} = 17\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 100\text{V}$
Reverse Recovery Charge	$Q_{rr}$	-	7.6	-	$\mu\text{C}$	
Reverse Recovery Current	$I_{rrm}$	-	32.5	-	A	

**■ Characteristic Graph**
**Fig.1 On-Region Characteristics.**

**Fig.2 On-Resistance Variation with Drain Current and Gate Voltage**

**Fig.3 On-Resistance Variation with Temperature (Normalized)**

**Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)**

**Fig.5 Transfer Characteristics**

**Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature**


**Fig.7 Gate Charge Characteristics**

**Fig.8 Capacitance Characteristics**

**Fig.9  $V_{GS(th)}$  Variation with Temperature (Normalized)**

**Fig.10 Maximum Drain Current vs. Case Temperature**

**Fig.11 Single Pulse Maximum Power Dissipation**

**Fig.12 Output Capacitance Stored Energy**


**Fig.13 Transient Thermal Response Curve**

**Fig.14 Maximum Safe Operating Area**


■ Test Circuit

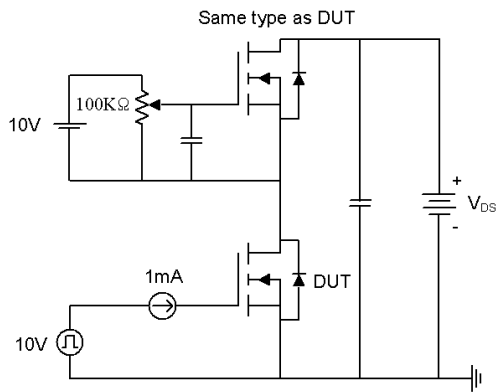


Fig15-1. Gate charge measurement circuit

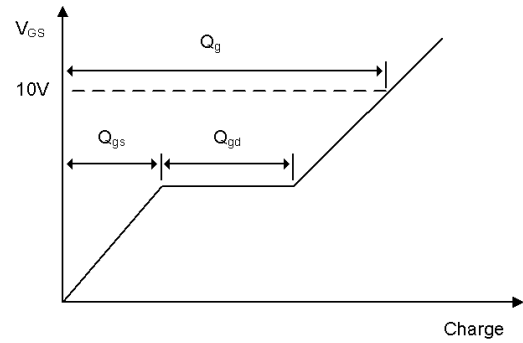


Fig15-2. Gate charge waveform

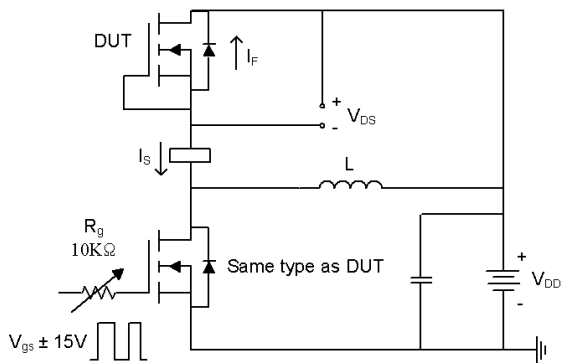


Fig16-1. Diode reverse recovery test circuit

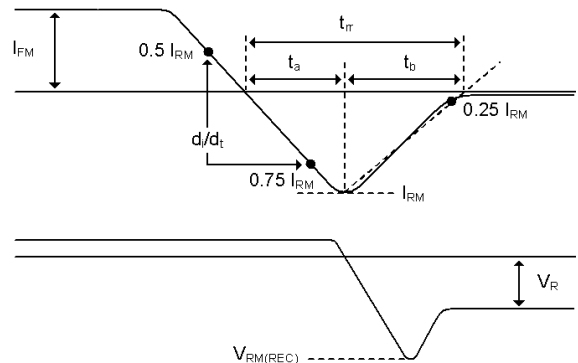


Fig16-2. Diode reverse recovery test waveform

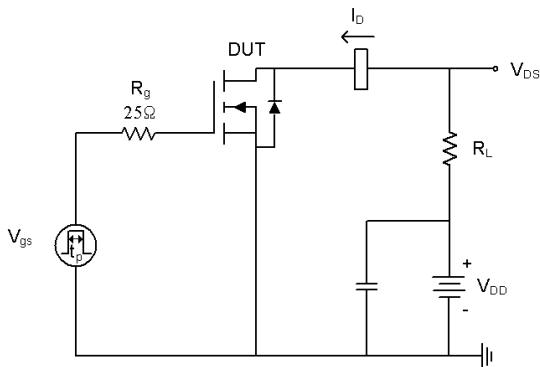


Fig17-1. Switching time test circuit for resistive load

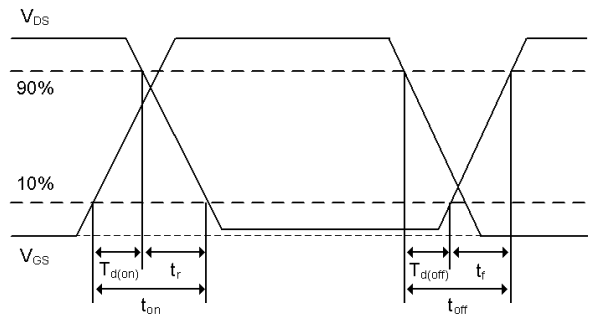


Fig17-2. Switching time waveform

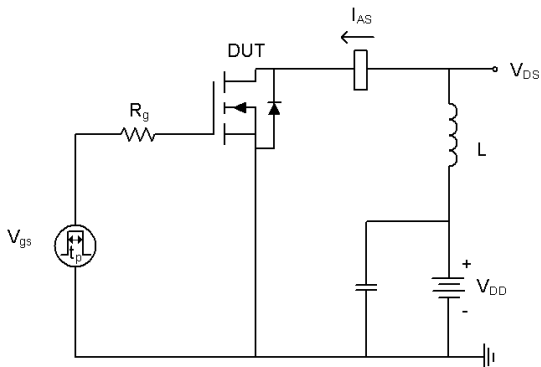


Fig18-1. Unclamped inductive load test circuit

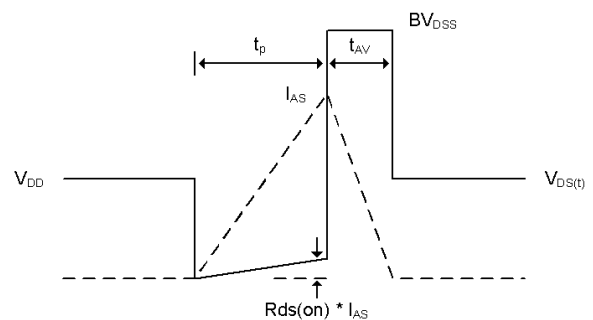
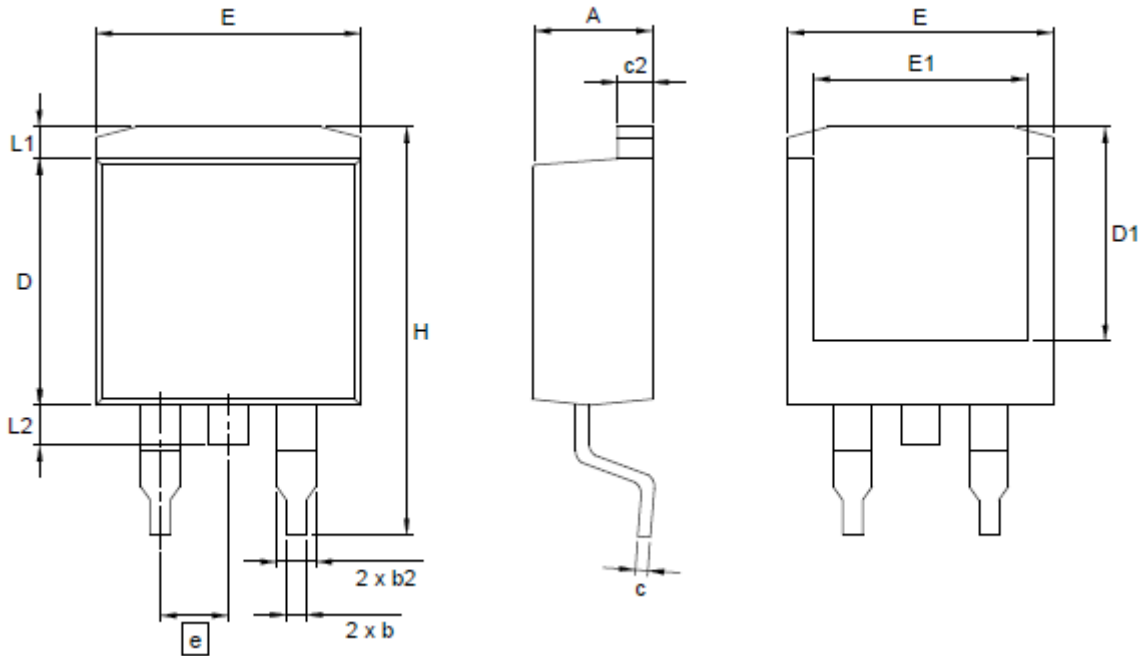


Fig18-2. Unclamped inductive waveform




**■ Physical Dimension**
**D<sup>2</sup>PAK(TO-263)**


**Note : Package body size, length and width do not include mold flash, protrusions and gate burrs.**

Symbol	Dimension (mm)		
	Min	Nom	Max
A	4.064	-	4.826
A1	-	-	0.254
b	0.508	-	0.99
b2	1.140	-	1.778
c	0.310	-	0.736
c2	1.140	-	1.650
D	8.382	-	9.652
D1	6.6	-	-
E	9.652	-	10.668
E1	6.223	-	-
e	BSC 2.54		
H	14.605	-	15.875
L	1.778	-	2.794
L1	-	-	1.676
L2	-	-	1.778
L3	BSC 0.254		

**DISCLAIMER:**

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